● General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Features

■AEC-Q101 Qualified

■Low $R_{DS(ON)}$ to minimize conductive loss

■High GOX reliability

■Dual die in one package

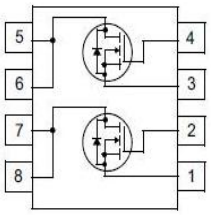
●Application

■BLDC Motor driver

■DC-DC

■Load switch

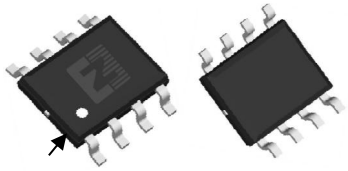
● Product Summary



V_{DS}= 60V

$R_{DS(ON)}$ = 55mΩ

I_D= 5A



SOP-8

●Ordering Information:

Part NO.	ZMDA68603S
Marking	ZMD68603
Packing Information	REEL TAPE
Basic ordering unit (pcs)	4000

●Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage	V_{GS}	Pulsed ①	20	V
Continuous Drain Current	I_D	T_C=25°C	5	A
	I_D	T_C=75℃	5	A
	I_D	T_C=100℃	4	A
Pulsed Drain Current	I_{DM}	Pulsed; tp < 10 μs; Tmb = 25°C	15	A
Total Power Dissipation	P_D	T_C=25℃	4	W
Total Power Dissipation	P_D	T_A=25℃	0.7	W
Operating Junction Temperature	T_J		-55 to +150	℃
Storage Temperature	T_{STG}		-55 to +150	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=10V, Rg=25Ω,	25	mJ
ESD Level (HBM)			CLASS 1C	

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	34	°C/W
Thermal resistance, junction-ambient②	R_{thJA}		-	180	°C/W
Soldering temperature	Tsold		-	260	°C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	1.3	1.7	2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 60V			1	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} =0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 6.5A		55	70	mΩ
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 6.5A			1.3	V

●Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	950		pF
Output capacitance	Coss		-	230	-	
Reverse transfer capacitance	Crss		-	113	-	
Gate Risistance	Rg	f = 1MHz	-	2		Ω
Total gate charge	Qg	V_{DD} = 15V，I_D = 20A V_{GS} = 10V	-	12	-	nC
Gate - Source charge	Qgs		-	2.4	-	
Gate - Drain charge	Qgd		-	3.2	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V，R_G =3.3Ω,I_D =20A	-	12	-	ns
Turn-ON Rise time	t_r		-	26	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	46	-	ns
Turn-Off Fall time	t_f		-	13	-	ns
Reverse Recovery Time	t_{RR}	V_{DD}=20V,dI_S/dt = 100A/us,I_S=50A	-	15	-	ns
Reverse Recovery Charge	Q_{RR}		-	16	-	nC

Fig.1 Gate-Charge Characteristics

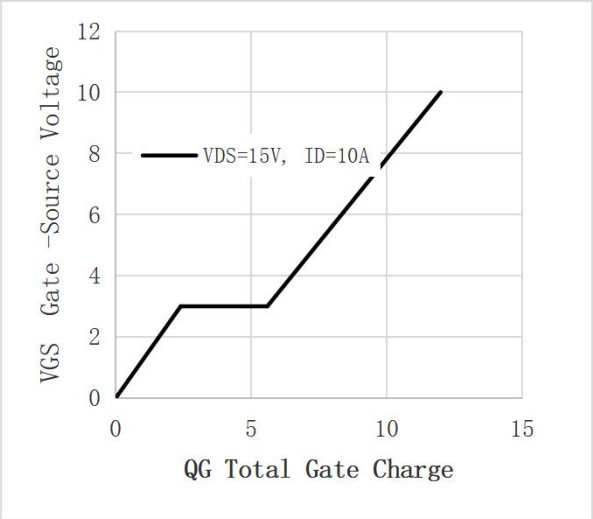


Fig.2 Capacitance Characteristics

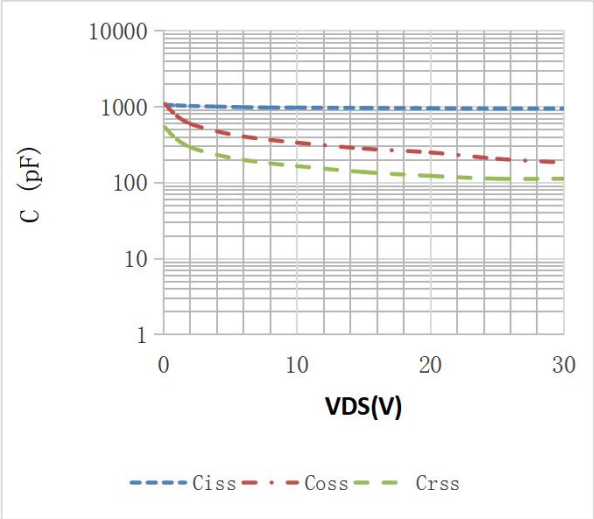


Fig.3 Power Dissipation

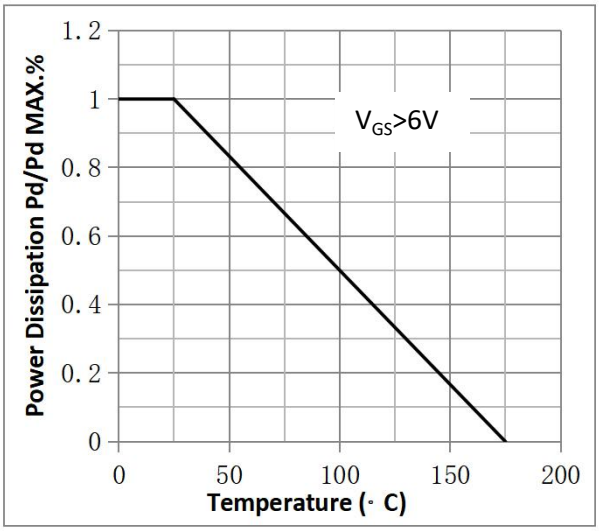


Fig.4 Typical output Characteristics

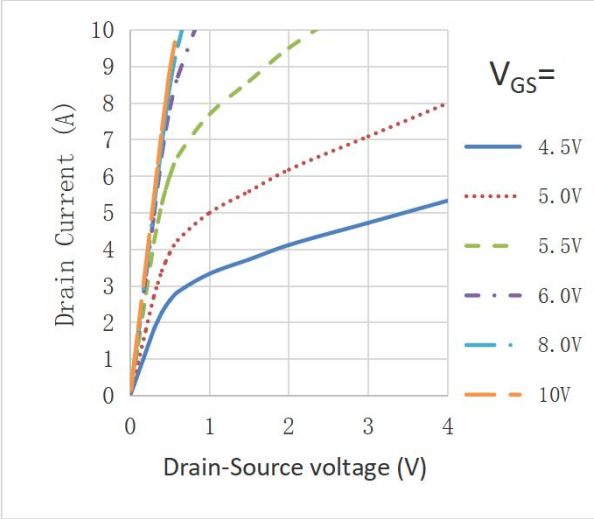


Fig.5 Threshold Voltage V.S Junction Temperature

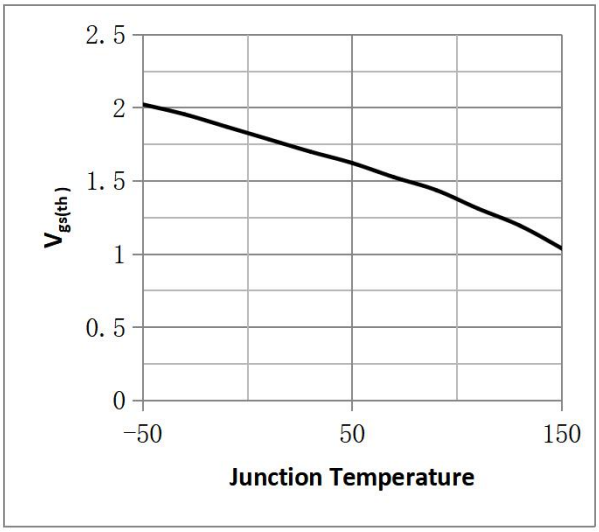


Fig.6 Resistance V.S Drain Current

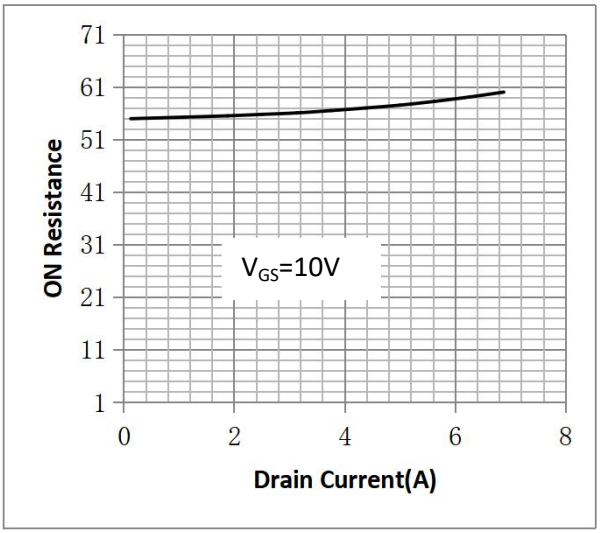


Fig.7 On-Resistance VS Gate Source Voltage

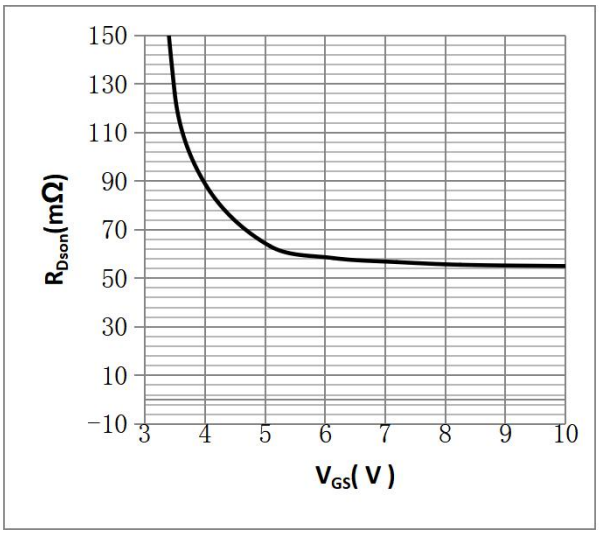


Fig.8 On-Resistance V.S Junction Temperature

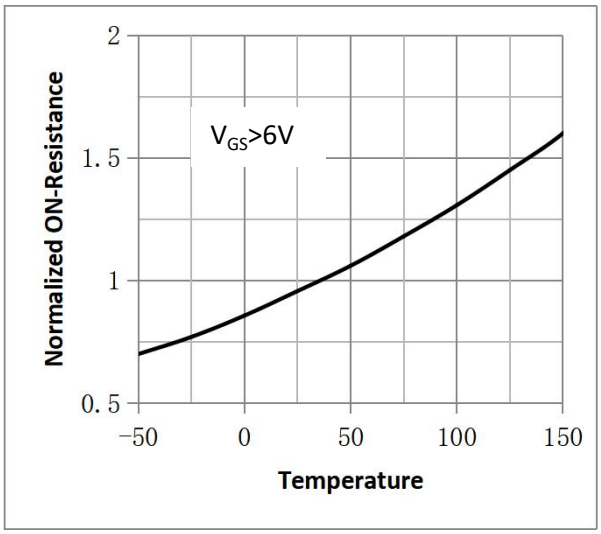


Figure 9. Diode Forward Voltage vs. Current

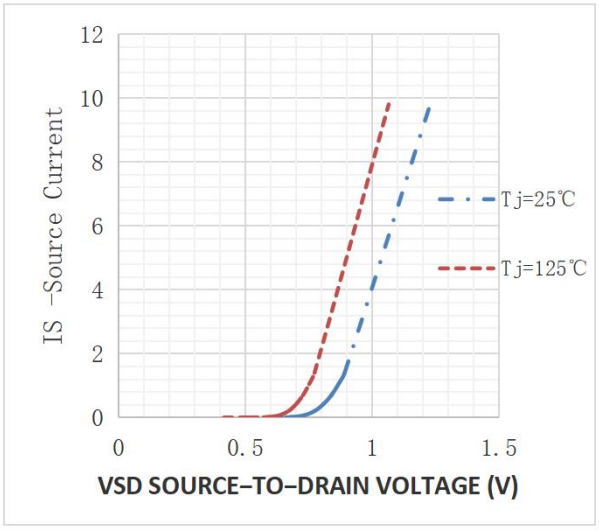


Figure 10. Transfer Characteristics

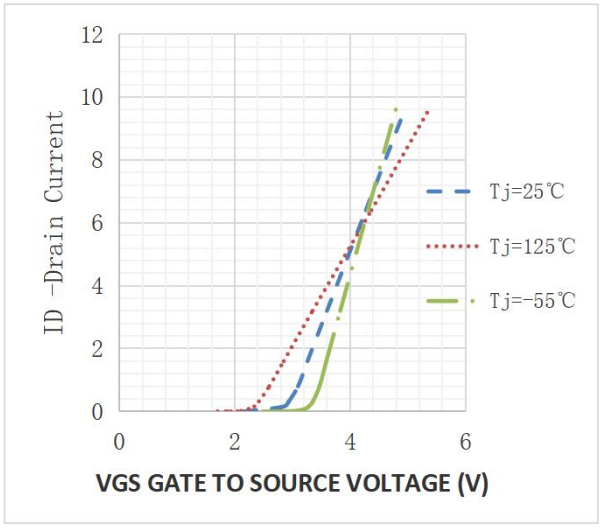


Fig.11 Safe Operating Area

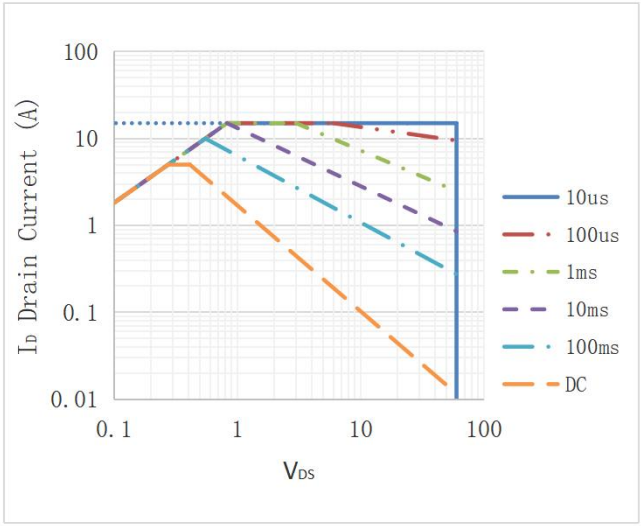
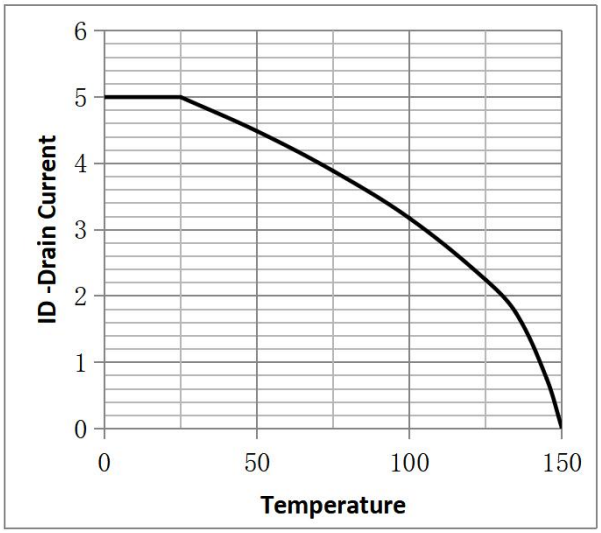
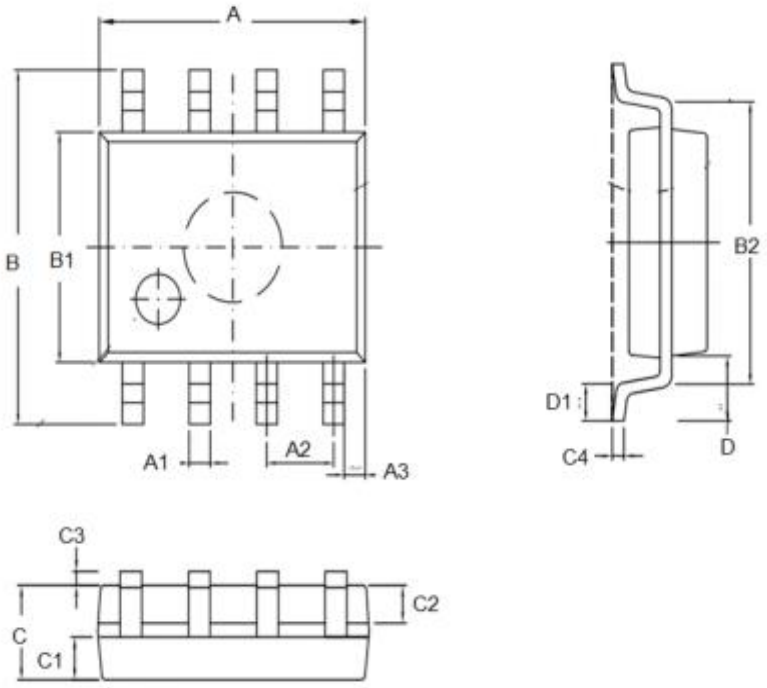


Fig.12 ID vs. Junction Temperature



●SOP-8 Package Outline

SYMBOL	min	TYP	max	SYMBOL	min		max
A	4.8		5.25	C	1.3		1.75
A1	0.37		0.49	C1	0.55		0.75
A2		1.27		C2	0.55		0.65
A3		0.41		C3	0.05		0.2
B	5.8		6.2	C4	0.1	0.2	0.23
B1	3.8		4.1	D		1.05	
B2		5		D1	0.4		0.62



Note:

① Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%, Accumulation time ≤50 hours; For DC， the following test conditions can be passed: VGS=+15V/-5V, Tj=150℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

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Revision History

Version	Date	Change
A	2021.2.16	NEW
B	2022.5.12	Modifyied the ID curve